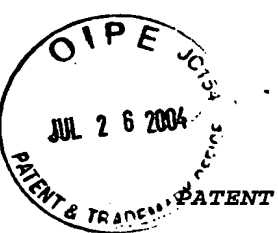


2123
epw



☒ OFFICIAL
☐ UNOFFICIAL

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): J. G. Walacavage et al.

Serial No: 09/965,905

Group Art Unit: 2123

Filed: September 28, 2001

Examiner: Not Assigned

Title: METHOD OF PART FLOW MODEL FOR PROGRAMMABLE LOGIC CONTROLLER LOGICAL VERIFICATION SYSTEM

<input checked="" type="checkbox"/> CERTIFICATE OF MAILING/TRANSMISSION (37 C.F.R. § 1.8(a))	
I hereby certify that this correspondence is, on the date shown below, being:	
MAILING	FACSIMILE
<input checked="" type="checkbox"/> deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450	<input type="checkbox"/> transmitted by facsimile to the Patent and Trademark Office
	Fax No: _____
	Total No. of Pages: _____
Date: <u>July 22, 2004</u>	<u>Daniel H. Bliss</u> Daniel H. Bliss

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

STATUS LETTER

Sir:

The above-identified patent application has been on file with the United States Patent and Trademark Office for more than one year and no office actions have been received. Attorney for Applicants request the status of this application including the name and telephone number of the Examiner.

Respectfully submitted,
By: Daniel H. Bliss
Daniel H. Bliss
Registration No. 32,398
Attorney for Applicant(s)

Date: July 22, 2004
Bliss McGlynn, P.C.
2075 West Big Beaver Road, Suite 600
Troy, Michigan 48084
(248) 649-6090

Ford Disclosure No. 200-0664